Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A device structure comprising:

a first transistor including a first gate electrode with a vertical ~~exterior~~ sidewall, a first gate dielectric disposed on the vertical ~~exterior~~ sidewall of said first gate electrode, ~~at least one~~ a plurality of first semiconducting carbon ~~nanotube~~ nanotubes each having a first end, a second end, and a channel region between said first and second ends and disposed adjacent to said first gate dielectric on said vertical ~~exterior~~ sidewall of said first gate electrode, a first source/drain contact electrically coupled with said first end of ~~said at least one~~ each of the first semiconducting carbon ~~nanotube~~ nanotubes, and a second source/drain contact electrically coupled with said second end of ~~said at least one~~ each of the first semiconducting carbon ~~nanotube~~ nanotubes;

a second transistor including a second gate electrode with a vertical ~~exterior~~ sidewall, a second gate dielectric disposed on the vertical ~~exterior~~ sidewall of said second gate electrode, ~~at least one~~ a plurality of second semiconducting carbon ~~nanotube~~ nanotubes each having a first end, a second end, and a channel region between said first and second ends and disposed adjacent to said second gate dielectric on said vertical ~~exterior~~ sidewall of said second gate electrode, a third source/drain contact electrically coupled with said first end of ~~said at least one~~ each of the second semiconducting carbon ~~nanotube~~ nanotubes, and a fourth source/drain contact electrically coupled with said second end of ~~said at least one~~ each of the second semiconducting carbon ~~nanotube~~ nanotubes~~, said vertical exterior sidewall of said second gate electrode separated from said vertical exterior sidewall of said first gate electrode by a space~~; and

a fill layer composed of a dielectric material and disposed ~~in said space~~ between said second gate dielectric on said vertical sidewall of said second gate electrode separated from said first gate dielectric on said vertical sidewall of said first gate electrode,

wherein ~~said first source/drain contact of said first transistor is aligned with said exterior sidewall of said first gate electrode, and~~ said ~~at least one~~ each of the first semiconducting carbon

~~nanotube~~ nanotubes is positioned in ~~said dielectric material within said space~~ between said second gate dielectric on said vertical sidewall of said second gate electrode and said first gate dielectric on said vertical sidewall of said first gate electrode, and portions of the dielectric material of said fill layer are disposed between adjacent pairs of the plurality of first semiconducting carbon nanotubes and between adjacent pairs of the plurality of second semiconducting carbon nanotubes.

2. (Cancelled)

3. (Currently Amended) The device structure of claim 1 wherein said ~~said at least one~~ the first semiconducting carbon ~~nanotube is~~ nanotubes are a single-wall semiconducting carbon nanotube.

4. (Cancelled)

5. (Currently Amended) The device structure of claim 1 wherein said first source/drain contact includes a catalyst pad characterized by a catalyst material having a composition effective for growing ~~said at least one~~ the first semiconducting carbon ~~nanotube~~ nanotubes.

6. (Currently Amended) The device structure of claim 5 wherein said first end of ~~said at least one~~ each of the first semiconducting carbon ~~nanotube is~~ nanotubes has a composition including the catalyst material or a material alloyed with the catalyst material.

7. (Previously Presented) The device structure of claim 1 wherein said first transistor further comprises:

an insulating layer disposed between said first source/drain contact and said first gate electrode for electrically isolating said first contact from said first gate electrode.

8. (Previously Presented) The device structure of claim 1 wherein said first transistor further comprises:

an insulating layer disposed between said second source/drain contact and said first gate electrode for electrically isolating said second source/drain contact from said first gate electrode.

9. (Withdrawn) The device structure of claim 1 wherein said first transistor further comprises:

a gate contact; and

at least one electrically-conducting carbon nanotube electrically coupling said first gate electrode with said gate contact.

10. (Withdrawn The device structure of claim 1 wherein said second source/drain contact includes a vertically-extending metal post electrically coupled with said second end of said at least one first semiconducting carbon nanotube.

11. (Withdrawn) The device structure of claim 10 wherein said second source/drain contact includes a conductive layer extending horizontally beneath said first gate electrode for electrically coupling said catalyst pad with said metal post.

12. (Withdrawn) The device structure of claim 1 wherein said second source/drain contact includes at least one electrically-conducting carbon nanotube extending substantially vertically and electrically coupled with said second end of each of said at least one first semiconducting carbon nanotube.

13. (Withdrawn) The device structure of claim 12 wherein said second source/drain contact includes a conductive layer extending horizontally beneath said first gate electrode for electrically coupling said second end of each of said at least one first semiconducting carbon nanotube with said at least one electrically-conducting carbon nanotube.

14-18. (Cancelled)

19. (Currently Amended) The device structure of claim 1 further comprising:

a substrate carrying said first and second transistors and characterized by a surface area viewed vertical to the substrate, and said ~~dielectric-filled~~ space ranges from about 20 percent to about 50 percent of said surface area.

20-33. (Cancelled)

34. (Previously Presented) The device structure of claim 5 wherein said catalyst pad further comprises nanocrystals of the catalyst material.

35. (Previously Presented) The device structure of claim 1 further comprising:

a capacitor electrically coupled with said first source/drain contact.

36. (Withdrawn) The device structure of claim 13 wherein said first transistor further comprises:

a catalyst pad electrically coupling said at least one electrically-conducting carbon nanotube with said conductive layer, said catalyst pad composed of a material capable of growing said electrically-conducting carbon nanotube.

37. (Withdrawn) The device structure of claim 36 wherein said catalyst pad further comprises nanocrystals of the catalyst material.

38. (Withdrawn) The device structure of claim 11 further comprising:

an insulating layer positioned between said conductive layer and said first gate electrode, said insulating layer electrically isolating said first gate electrode from said conductive layer.

39. (Withdrawn) The device structure of claim 11 further comprising:

a substrate carrying said first and second transistors, said conductive layer being arranged vertically between said first gate electrode and said substrate.

40. (Withdrawn) The device structure of claim 13 further comprising:

an insulating layer positioned between said conductive layer and said first gate electrode, said insulating layer electrically isolating said first gate electrode from said conductive layer.

41. (Withdrawn) The device structure of claim 13 further comprising:

a substrate carrying said first and second transistors, said conductive layer being arranged vertically between said first gate electrode and said substrate.

42. (Withdrawn) The device structure of claim 9 wherein said first transistor further comprises:

a catalyst pad electrically coupling said electrically-conducting carbon nanotube with said first gate electrode, said catalyst pad participating in the synthesis of said electrically-conducting carbon nanotube.

43-54. (Cancelled)

55. (Previously Presented) The device structure of claim 1 wherein said first transistor and said second transistor are formed on a substrate, and further comprising:

a conductive layer disposed between said first source/drain contact of said first transistor and the substrate.

56. (Previously Presented) The device structure of claim 55 wherein said conductive layer is disposed between said first source/drain contact of said second transistor and the substrate.

57. (Previously Presented) The device structure of claim 55 wherein further comprising:

an insulating layer disposed between said first gate electrode and said conductive layer.

58. (Cancelled)